EXPANDING ADC1 DYNAMIC RANGE FOR THE Si8250

1. Introduction

The Si8250 data sheet specifies a common mode input range of 0.6 to 1.2 V for ADC1. This range effectively limits the dynamic voltage output range in voltage-controlled converters. For example, the output range for a 3.3 V power supply designed to generate a 1.00 V sense would have an absolute maximum dynamic range of 1.98 to 3.96 V. In reality, the active regulation point would need to be something greater than 1.98 V and less than 3.96 V since these are on the very fringes of the common mode specification. If a design requires wider dynamic output voltage range (e.g., 2.00–5.70 V) then a simple resistor divider will not work. This application note discusses a simple and inexpensive solution to expand the dynamic range for applications such as power factor correction and wide variable output power supplies.

2. ADC1 Common Mode Limits

The specified common mode range for ADC1 (Figure 1) is from 0.6 V to the voltage reference which is typically 1.2 V. This simply means that the input voltages to ADC1 from both V_{SENSE} and the REFDAC should stay within the range of 0.6 to 1.2 V referenced to the common ground to achieve good linear response. For input voltages much lower than the common mode specification, ADC1 exhibits non-linear characteristics. Figure 2 shows an example of the ADC1 dc response when the inputs are significantly out of specification. For input voltages above the common mode range the input is effectively “cut off” yielding no change in the ADC output.

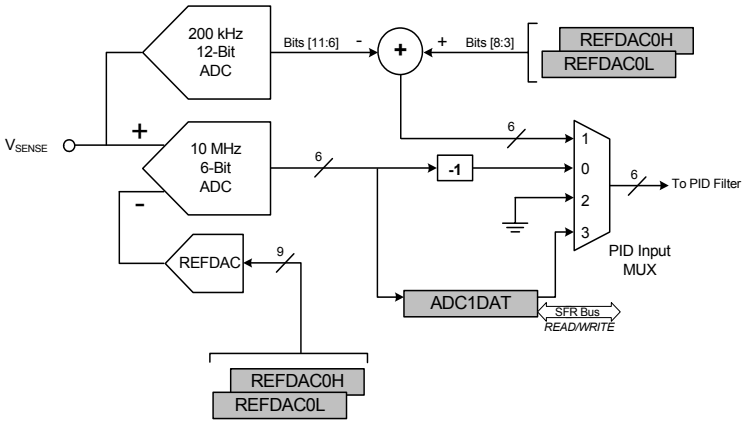

Figure 1. ADC1 Block Diagram

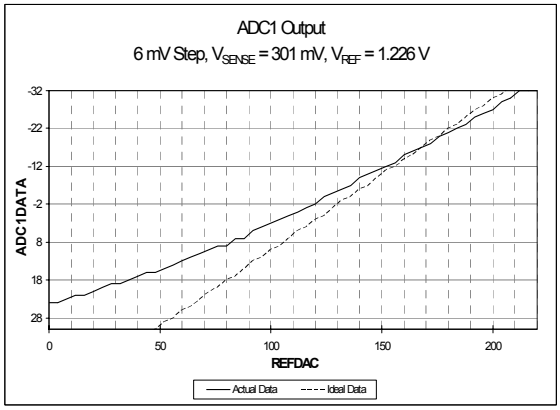

Figure 2. ADC1 Results Below the Common Mode Specification

3. Dynamic Range Limit

The simplest and most economical feedback approach is to divide the output voltage with a simple resistor divider as shown in Figure 3.

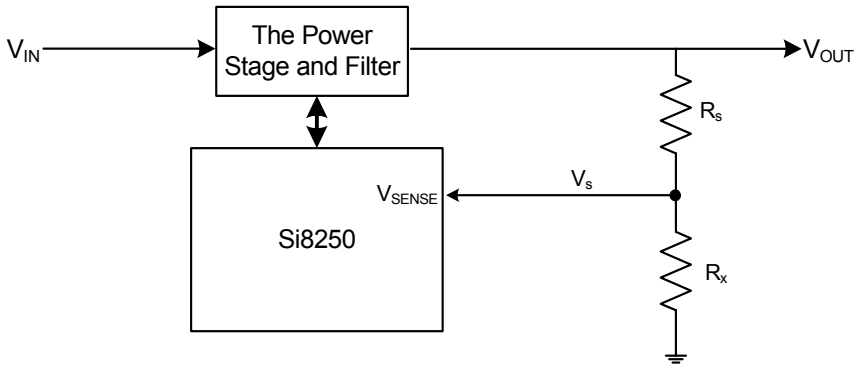

Figure 3. Resistor Divider

Thus, the output voltage is proportional to the inverted resistor divider ratio, Equation 2, times the sense voltage as shown in Equation 1. For simplicity, the inverted resistor divider ratio from this point forward will be referred to as the α ratio.

$$V_o = \alpha V_s$$

Equation 1. Output Voltage/Sense Voltage Relation

$$\alpha = \frac{R_s + R_x}{R_x}$$

Equation 2. Inverted Resistor Divider Ratio

Similarly, it is easily shown that the range of the output voltage is proportional by the α ratio to the range of the sense voltage, and this is where fundamental limits can be seen. The range of the sense voltage is bounded by the common mode input specification, $\Delta Vs = 1.2–0.6\ V = 0.6\ V$.

$$V_{oh} - V_{ol} = \alpha V_{sh} - \alpha V_{sl} \quad \rightarrow \quad \Delta V_o = \alpha \Delta V_s$$

Equation 3. Output / Sense Dynamic Range Relation

For example, the operating range for a particular design is 2.2 to 5.5 V with 200 mV of operating margin on either side. Thus, the absolute range of the supply is defined to be 2.0 to 5.7 V. However, starting with the minimum sense voltage at the minimum output voltage, the maximum achievable output voltage is 2.0 V + $\alpha\Delta Vs$ = 4.0 V. At an output of 4.0 V, the sense voltage is at its maximum limit of 1.2 V. This graphical relationship is shown in Figure 4. Thus the desired 5.7 V maximum range is not achievable with the feedback circuit shown in Figure 3.

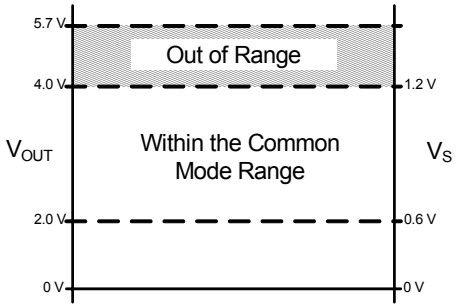

Figure 4. Output Voltage Limit

4. Expanding the Dynamic Range

To dynamic range may be expanded by allowing the α ratio in Equation 1 and Equation 3 to be variable. This is accomplished by changing the value of R_x in Figure 3. One solution is to connect parallel resistors to port pins on the Si8250 as shown in Figure 5. To change the α ratio, drive one of the connected port pins low to engage a parallel resistance or allow the pin to float (high impedance) to disengage a parallel resistance.

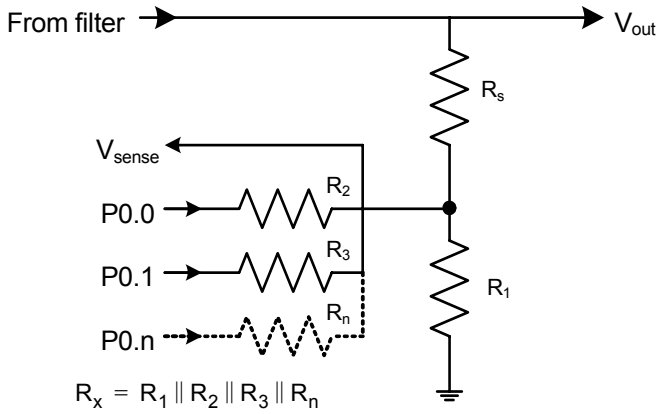

Figure 5. Feedback with Common Mode Compensation

4.1. Adding Margin to the Common Mode Limits

It is important to add margin to the common mode limits to ensure that ADC1 is not converting at the boundary of the common mode range. Operating at the boundary ultimately affects the transient response performance. For example, if the reference DAC shown in Figure 1 is set to deliver a 1.17 V signal to ADC1, this would leave 30 mV operating margin for ADC1 Vs (min). In a situation where ADC1 is set to deliver a 6 mV resolution, 30 mV is only 5 LSB. Thus, if a positive going transient were to occur, the maximum possible error from ADC1 would be 5 LSBS. Thus, the loop response is asymmetrical in this example. The bandwidth is severely limited for positive transients (up to 5 LSB), while the bandwidth for negative going transients would be limited only by the maximum dynamic range of ADC1 (up to 32 LSB).

Therefore, it is necessary to calculate the operating limits set by deciding the maximum allowed transient *m* (LSB). The α ratios and resistor values are determined based on these operating limits. Equation 4 defines the minimum sense voltage Vs (min) and Equation 5 defines the maximum sense voltage Vs (max). In these equations V_{step} is the resolution of ADC1 (mv), and V_{com} is the common mode voltage.

$$V_{s(min)} = V_{com(min)} + m(V_{step}) \rightarrow V_{s(min)} = 0.6V + m(V_{step})$$

Equation 4. Minimum Sense Voltage

$$V_{s(max)} = V_{com(max)} - m(V_{step}) \rightarrow V_{s(max)} = 1.2V - m(V_{step})$$

Equation 5. Maximum Sense Voltage

4.2. Determining the α Ratios

As shown earlier in Equation 2, the α ratio is defined by the resistor divider. As shown in Figure 5, there will be some number of resistors that will be used to adjust the ratio. The α ratios must be determined to find the number of resistors and their values for the circuit shown in Figure 5. Equation 6 and Equation 7 are used to determine the α ratios and peak voltages for these ratios.

Equation 6 is a recursive function that relates the previous maximum output voltage V(n–1) to the next maximum output voltage V(n) for a given α ratio. Each voltage step represents the maximum output voltage that can be achieved for a particular α ratio. It is derived by relating the maximum output voltage for one α ratio to the minimum output of the next ratio.

Equation 7 is essentially the same as Equation 2 written in another form. It provides the α ratio for the calculated maximum voltage provided by Equation 6.

Each successive maximum voltage is calculated with Equation 6. Start from the minimum voltage of the desired range, and iterate Equation 6 until the voltage exceeds the desired maximum output voltage. The number of iterations determine the number of resistors needed to achieve the desired voltage range.

For each iteration of Equation 6 an α ratio can be calculated with Equation 7. The α ratio will be used in the next section to determine the resistor values.

$$V_n = V_{n-1}\frac{V_{s(max)}}{V_{s(min)}} \quad \text{where} \quad V_0 = V_{out(min)}$$

Equation 6. Max Output Steps

$$\alpha_n = \frac{V_n}{V_{s(min)}}$$

Equation 7. The Alpha Ratio for a Given Peak Output

For example, as used previously, the desired operating range is from 2.0 to 5.7 V. Equation 6 is iterated three times yielding a maximum voltage of 8.4 V, which exceeds the 5.7 V requirement. Then the three α ratios are calculated. The α ratios for this example are presented graphically in Figure 6. Therefore, the circuit in Figure 5 only requires three resistors to achieve the desired 2.0 to 5.7 V operating range. The exact resistor values are calculated in “4.3. Determining the Parallel Resistors”.

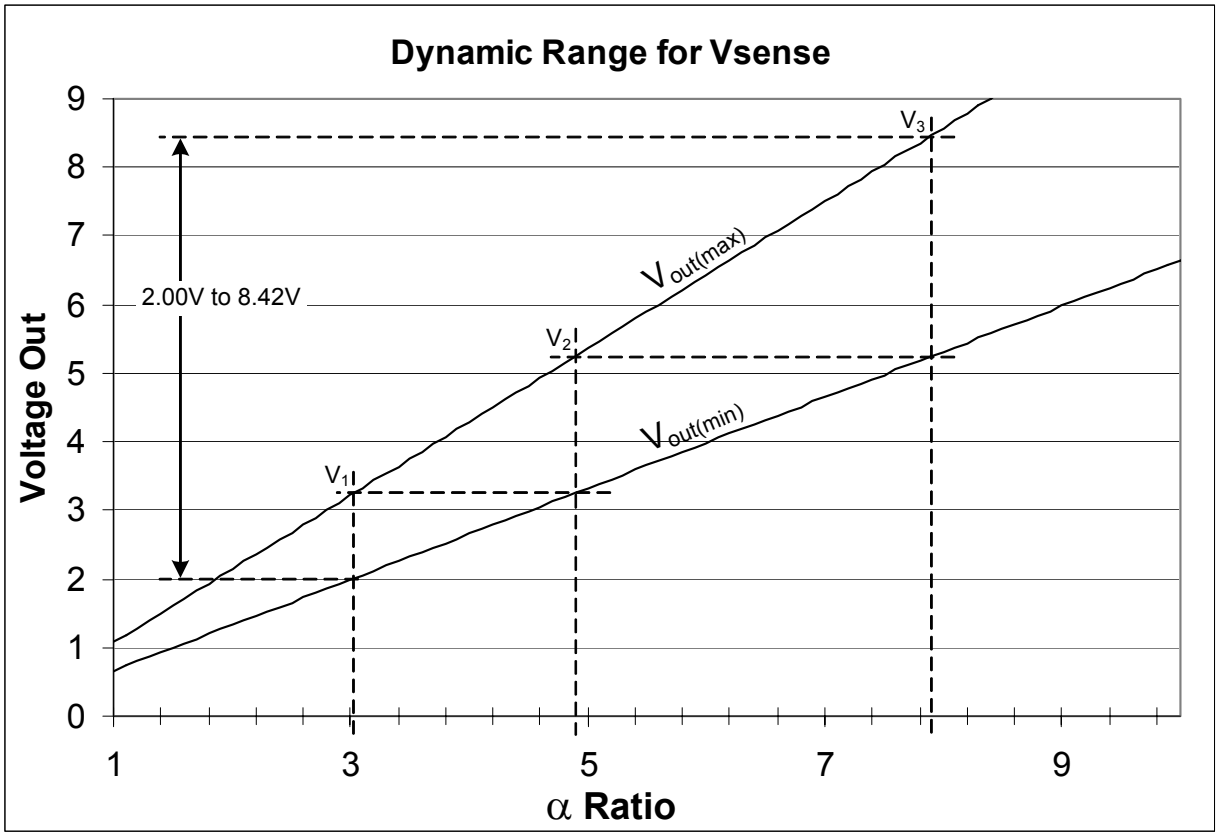

Figure 6. Graphical Determination of the α Ratios

4.3. Determining the Parallel Resistors

Once the α ratios are determined, they must be decomposed to individual resistor values. The equivalent resistance, R_{xn}, is calculated from the associated α ratio. Equation 8 gives these resistances for each successive R_{xn}. Note that R_{xn} represents the equivalent resistance, which is a composition of parallel resistors.

$$R_{xn} = \frac{R_s}{\alpha_n - 1}$$

Equation 8. The Equivalent Resistance

Equation 9 defines R_{xn} as a cascade of parallel resistors where *n* represents the sequence of parallel resistors. For example, R_{x2} is the equivalent resistance of R_1 in parallel with R_2.

$$R_{xn} = R_1 \| R_2 \| R_3 \| \ldots \| R_n$$

Equation 9. Parallel Resistance

The individual resistor values are extracted from Equation 10.

$$R_n = \frac{R_{xn-1} R_{xn}}{R_{xn-1} - R_{xn}}$$

Equation 10. The Resistor In Terms of the Previous and Current Parallel Resistance

4.4. Design Example

An output range from 2.0 to 5.7 V is desired for a particular power supply (this example is used quite often throughout this application note). The high-side margin is specified to be 32 LSB, and the low-side margin is specified to be 16 LSB. The ADC resolution is set at 4 mV. These settings yield a sense voltage range of 0.664 to 1.072 V. The high-side resistor, R_s, is specified to be 7500 Ω. The results are easily calculated with a spreadsheet and are shown in Figure 7. The resulting circuit is shown in Figure 8.

Parameter	Value	Unit
Vout(min)	2.00	V
Vcom(min)	0.60	V
Vcom(max)	1.20	V
Low offset	16	LSB
High offset	32	LSB
Step size	0.004	V
Rs	7500	ohms
Vs(min)	0.664	V
Vs(max)	1.072	V

n	αn	Vn	Rxn	Rn
1	3.01	3.23	3727.54	3727.54
2	4.86	5.21	1941.58	4052.35
3	7.85	8.42	1094.76	2510.04
4	12.67	13.59	642.41	1554.73
5	20.46	21.94	385.35	963.00
6	33.04	35.42	234.11	596.49
7	53.34	57.18	143.30	369.47

Figure 7. Example Spreadsheet Calculations for a Wide Dynamic Output

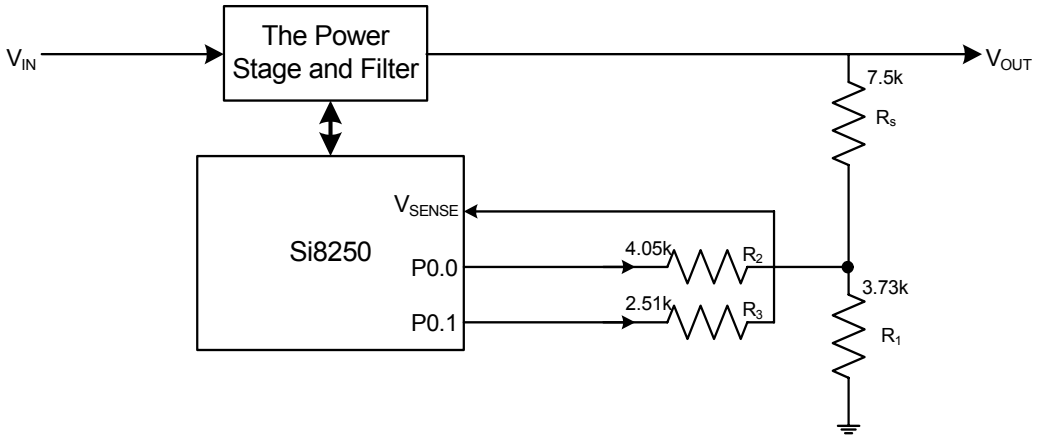

Figure 8. The Example Voltage Sense Circuit

5. Code Overview

Code must also be developed to manipulate the port pins and accommodate the wider operating range. In essence, the desired output is checked against the threshold range, and the corresponding port pins are driven accordingly. Each pin can be driven low to engage the resistor, thus raising the peak output voltage. Or each pin can be allowed to float, thus lowering the peak output voltage. For each range, the REFDAC output also must be changed to correspond to the appropriate output voltage range. This operation is best described in a program flow example. Figure 9 shows the program flow that could be used to change the output voltage for the example described in “4.4. Design Example”.

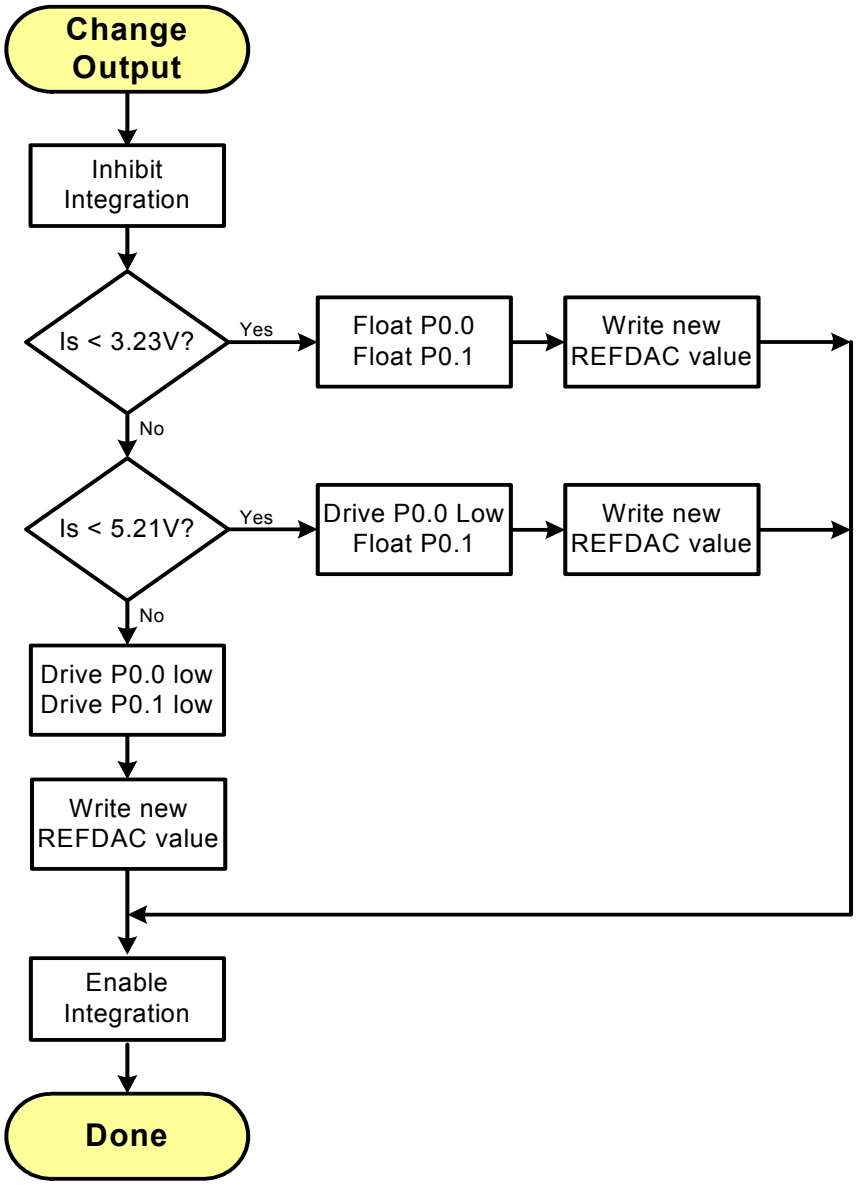

Figure 9. Program Flow Example

5.1. A Code Example

Coding the flowchart shown in Figure 9 can be accomplished in many forms, the code discussed here and presented below is just one example.

A parameter representing the desired output voltage is passed in. The range of the parameter is specified from 0 to 10 V, which includes the desired range of 2.0 to 5.7 V with more than sufficient resolution. Next, the desired range is decoded from the request. (i.e., in the example, “4.4. Design Example”, is the output within the 2.00–3.23 V, 3.23–5.21 V, or 5.21–8.42 V range?) Once the range is decoded the scaled REFDAC value is calculated and stored in a temporary location. Also the resistor settings are stored in a temporary location. The loop is briefly opened while the settings are written (REFDAC and resistors); then the loop is closed again.

```
// This function sets the output voltage. The 16-bit parameter 'vout'
// represents a voltage between 0V and 10V. The output ranges are as
// follows:
//           Voltage range       Scale Factor     RES2   RES3
//           2.00V - 3.23V       46               1      1
//           3.23V - 5.21V       75               1      0
//           5.21V - 8.42V       121              0      0
//
// The scale factor is calculated from the following equation:
// scale factor = Vn * Vref * 65535 / 10 / Vs(max) / 511
void SetVout(unsigned int vout)
{
   unsigned int _temp;
   bit _tempR2;
   bit _tempR3

   // If the desired output is less than 3.23V
   if (vout < 0x522D) {
      // Float both resistors
      _tempR2 = 1;
      _tempR3 = 1;

      // Scale the internal voltage to the real voltage
      _temp = vout / 46;
   } else

   // If the desired output is less than 5.21V
   if (vout < 0x8560) {
      // Tie RES2 to ground and float RES3
      _tempR2 = 0;
      _tempR3 = 1;

      // Scale the internal voltage to the real voltage
      _temp = vout / 75;
   } else

   // Otherwise the output is less that 8.42V
   {
      // Tie both resistors to ground
      _tempR2 = 0;
      _tempR3 = 0;

      // Scale the internal voltage to the real voltage
      _temp = vout / 121;
   }

   // Set the resistors
   RES2 = _tempR2;
   RES3 = _tempR3;

   // Write to the REFDAC
   REFDAC0H = _temp >> 8;
   REFDAC0L = _temp;

   // Clear the integrator
   PIDKICN |= 0x80;
   PIDKICN &= ~0x80;
}
```

6. Summary

Although ADC1 on the Si8250 does have a specified common mode range; this does not necessarily limit the dynamic range of the output of a voltage controlled power supply. As described in this application note, it is relatively easy and inexpensive to add dynamic range programming with just a few extra resistors and some code.

CONTACT INFORMATION

Silicon Laboratories Inc.

4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: MCUinfo@silabs.com
Internet: www.silabs.com

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